CLAIMS

What is claimed is:

1. A successive approximation analog-to-digital converter comprising:

an analog sample and hold circuit;

a switched capacitor DAC having an input coupled to an output of the sample and hold circuit;

a comparator having an input coupled to an output of the switched capacitor DAC;

a plurality of set-reset latches, each set-reset latch being responsive to a combination of control signals and the output of the comparator and providing non-overlapping switch driver signals as set-reset latch outputs;

the switch driver signals being coupled to control the switched capacitor DAC.

2. The converter of claim 1 wherein the switched capacitor DAC is a differential switched capacitor DAC.

3. The converter of claim 1 further comprised of a controller coupled to provide the control signals.

4. The converter of claim 3 wherein the controller is a state machine.

5. The converter of claim 1 wherein the set-reset latches have switch driver signal outputs that are level shifted in comparison to the combination of control signals and the output of the comparator.

6. The converter of claim 1 wherein the set-reset latches are NOR gate based latches.

7. The converter of claim 1 wherein the set-reset latches are NAND gate based latches.

8. The converter of claim 1 wherein the set-reset latches are hybrid logic gate based latches.

9. The converter of claim 1 wherein the switched capacitor DAC is a binary coded DAC.

10. The converter of claim 1 wherein the switched capacitor DAC is a reduced radix DAC.

11. The converter of claim 1 wherein the switched capacitor DAC is a mixed radix DAC.

12. A successive approximation analog-to-digital converter comprising:

an analog sample and hold circuit;

a differential switched capacitor DAC having an input coupled to an output of the sample and hold circuit;

a comparator having an input coupled to an output of the switched capacitor DAC;

a plurality of set-reset latches, each set-reset latch being responsive to a combination of control signals and the output of the comparator and providing non-overlapping switch driver signals as set-reset latch outputs; and,

a controller coupled to provide the control signals;

the switch driver signals being coupled to control the switched capacitor DAC.

13. The converter of claim 12 wherein the set-reset latches have latch outputs that are level shifted in comparison to the combination of control signals and the output of the comparator.

14. The converter of claim 12 wherein the set-reset latches are NOR gate based latches.

15. The converter of claim 12 wherein the set-reset latches are NAND gate based latches.

16. The converter of claim 12 wherein the set-reset latches are hybrid logic gate based latches.

17. The converter of claim 12 wherein the switched capacitor DAC is a binary coded DAC.

18. The converter of claim 12 wherein the switched capacitor DAC is a reduced radix DAC.

19. The converter of claim 12 wherein the switched capacitor DAC is a mixed radix DAC.

20. In a successive approximation analog-to-digital converter, the improvement comprising:

a plurality of combined set-reset latches and switch drivers responsive to a combination of control signals and the output of a comparator to provide successive approximation switch signals to a switched capacitor DAC, each combined set-reset latch and switch driver having a set-reset latch having switch driver signals as latch outputs.

21. The improvement of claim 20 wherein the set-reset latches having switch driver signals as latch outputs have latch outputs that are level shifted in comparison to the inputs to the set-reset latches.

22. A method of providing latched non-overlapping switch driver signals comprising:

providing a set-reset latch responsive to latch control signals referenced to a first voltage;

powering the latch at a second voltage different than the first voltage;

coupling non-overlapping signals within the set-reset latch as non-overlapping switch driver signal outputs.

23. The method of claim 22 wherein the second voltage is higher than the first voltage.

24. The method of claim 22 wherein the non-overlapping signals are non-overlapping in the positive logic sense.

25. The method of claim 22 wherein the non-overlapping signals are non-overlapping in the negative logic sense.

26. The method of claim 22 wherein the non-overlapping signals comprise two non-overlapping signals in the positive logic sense and two non-overlapping signals in the negative logic sense.